Remarks

In the present response, claims 1-22 are presented for examination.

I. Claim Rejections: 35 USC § 102(b)

Claims 1-3, 5-6, 10-15, and 17-20 are rejected under 35 USC § 102(b) as being anticipated by USPN 5,717,648 (Davis). Applicants respectfully traverse this rejection.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Davis neither teaches nor suggests each element in the rejected claims, these claims are allowable over Davis.

Claim 1

Independent claim recites numerous recitations that are not taught or suggested in Davis. By way of example, claim 1 recites an integrated circuit device having three separate elements: a memory array, a decoder, and a cache. Davis does not teach or even suggest an integrated circuit that has each of these three separate elements. As shown in FIG. 1, Davis teaches a single integrated circuit chip 10 that has a cache 40, a CPU 20, a memory management unit 30, and a bus unit 24 (see Davis at 5: 41-44). Notice that the integrated circuit chip 10 does not include separate elements of a cache and a memory array.

The Office Action argues that claim 1 in Davis recites a memory array and FIG. 1 in Davis shows a cache. The Office Action further equates this memory array and this cache in Davis with two of the elements of Applicants' claim 1 (i.e., Applicants' claimed memory array and cache). Applicants respectfully state that this analysis is legally deficient. Claim 1 in Davis does recite a memory array. This memory array, however, is the same as Davis' cache. FIGS. 1 and 2 in Davis show a cache 40 as a large box. FIG. 3 in Davis shows the logic diagram of the cache of FIGS. 1 and 2 (See Davis at 6: 13-14). In other words, FIG. 3 merely shows a more detailed view of the cache. As shown in FIG. 3, the cache is the memory array (see Davis at 6: 14-15). This memory array is what Davis claims in his claim 1.

Applicants' claim 1 recites separate elements of a cache that is coupled to a memory array. In Davis, the memory array is the cache. Further, Applicants' claim 1 recites that "the cache is configured to retrieve data stored in the memory array in anticipation of a request for said data." This recitation is not possible in Davis given the interpretation of the Office Action. In other words, the cache 40 in Davis cannot be configured to retrieve data stored in a memory array because the cache and memory array in Davis are the same element. A cache is a memory array. Davis does not teach or even suggest two **different** elements of a cache and a memory array that are coupled together.

For at least these reasons, claim 1 and its dependent claims are allowable over Davis.

Claim 10

Claim 10 recites numerous recitations that are not taught or suggested in Davis. By way of example, claim 10 recites two different elements of a cache and memory cell array that are both integrated on a substrate. As noted above in connection with claim 1, Davis teaches an integrated circuit chip 10 that includes a cache 40. This circuit chip in Davis, however, does not include the separate elements of both a cache and a memory cell array. The cache in Davis is the memory cell array in Davis.

Applicants' claim 10 recites retrieving data from the memory cell "if the cache does not possess data associated with the address value." This recitation is not possible in Davis given the interpretation of the Office Action. In other words in Davis, data from the memory array 41 cannot be retrieved if the cache 40 does not possess the data because the cache and memory array in Davis are the same element. A cache is a memory array. Davis does not teach or even suggest two **different** elements of a cache and a memory array.

For at least these reasons, claim 10 and its dependent claims are allowable over Davis.

Claim 19

Claim 19 recites numerous recitations that are not taught or suggested in Davis. By way of example, claim 19 recites two different elements of a cache and memory cell array that are both integrated on a substrate. **The memory cell array is coupled to a separate cache.** As noted above in connection with claim 1, Davis teaches an integrated circuit chip 10 that includes a cache 40. This circuit chip in Davis, however, does not include the separate elements of both a cache and a memory cell array. The cache in Davis is the memory cell array in Davis.

For at least these reasons, claim 19 and its dependent claims are allowable over Davis.

II. Claims Rejection: 35 USC § 103(a)

Claim 4 is rejected under 35 USC § 103(a) as being unpatentable over Davis in view of USPN 6,628,598 (Edwards). Edwards fails to cure the deficiencies of Davis noted in section I. For at least these reasons, claim 4 is allowable.

III. Claims Rejection: 35 USC § 103(a)

Claims 7-9 and 22 are rejected under 35 USC § 103(a) as being unpatentable over Davis in view of USPN 6,163,477 (Tran) and USPN 4,099,266 (Biggers). Tran and Biggers fail to cure the deficiencies of Davis noted in section I. For at least these reasons, claims 7-9 and 22 are allowable.

IV. Claims Rejection: 35 USC § 103(a)

Claims 16 and 21 are rejected under 35 USC § 103(a) as being unpatentable over Davis in view of USPN 6,266,700 (Baker). Baker fails to cure the deficiencies of Davis noted in section I. For at least these reasons, claims 16 and 21 are allowable.

CONCLUSION

In view of the above, Applicants believe that all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. (832) 236-5529. In addition, all correspondence should continue to be directed to the following address:

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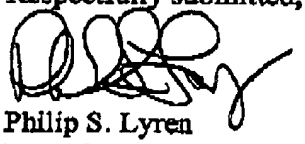
Respectfully submitted,



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CERTIFICATE UNDER 37 C.F.R. 1.8

The undersigned hereby certifies that this paper or papers, as described herein, is being transmitted to the United States Patent and Trademark Office facsimile number 571-273-8300 on this 18th day of May, 2006.

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